

# **STK8325**

# **Digital Output 3-axis MEMS Accelerometer**

# **Datasheet**

Version - 1.3

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Hazardous Substance Free

RoHS / REACH Compliant

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#### 1. OVERVIEW

#### **Description**

The STK8325 is a ±2g/±4g/±8g, 3-axis linear accelerometer, with digital output (I<sup>2</sup>C and SPI). It is a low profile capacitive MEMS sensor featuring, compensation for 0g offset and gain errors, and conversion to 12-bit digital values at user configurable samples per second. The device can be arranged for sensor data changes through the interrupt pins. The STK8325 is available in a small 2.0mm x 2.0mm x 1.0 mm LGA package and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

#### **Feature**

- Low Voltage Operation:
  - Supply Internal Domain Voltage: 1.7V~3.6V
  - I/O Voltage Range: 1.62V~3.6V
- ±2g/±4g±/8g dynamically selectable full-scale
- I<sup>2</sup>C digital output interface
- 3-wire and 4-wire SPI digital output
- 2 physical interrupts
- Low noise
- 12 bit data output
- 10000 g high shock survivability
- 2.0mm x 2.0mm x 1.0 mm LGA Package
- Configurable Samples from 14 to 2000 samples per second
- Sleep Feature for Low Power Consumption
- On-chip interrupt controller, motion-triggered interrupt-signal generation for
  - New data
  - Any-motion (slope) detection
  - Significant motion
- On-chip FIFO, integrated 32 frames FIFO buffer
- RoHS Compliant
- Halogen Free
- Environmentally Preferred Product
- Moisture Sensitivity Level 3

#### **Applications**

- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation
- Pedometer

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- Activity trackers for fitness apps
- Smart power management for mobile devices

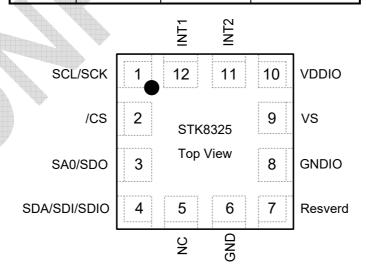


# 2. PIN DESCRIPTION

Pin#	Name	Dir.	Function
1	SCL/SCK	I	Serial Communications Clock (I <sup>2</sup> C, Open-Drain).
2	/CS	I	'0' for SPI mode and '1' or floating for I2C mode. SPI mode Chip Select.
3	SA0/SDO	I	I <sup>2</sup> C slave address selection pin, '1' for 0x1F and '0' for 0x0F. Serial Data Output (SPI 4-Wire)/ NC (SPI 3-Wire).
4	SDA/SDI/SDIO	В	Serial Data (I <sup>2</sup> C, Open-Drain). Serial Data Input (SPI 4-Wire). Serial Data Input and Output (SPI 3-Wire).
5	NC	NC	Not Internally Connected.
6	GND	GND	Must be connected to ground.
7	Reserved	I	Recommended tie to GND.
8	GNDIO	GND	Must be connected to ground.
9	VS	PWR	Supply Voltage.
10	VDDIO	PWR	Digital Interface Supply Voltage.
11	INT2	0	Interrupt 2 Output.
12	INT1	0	Interrupt 1 Output.

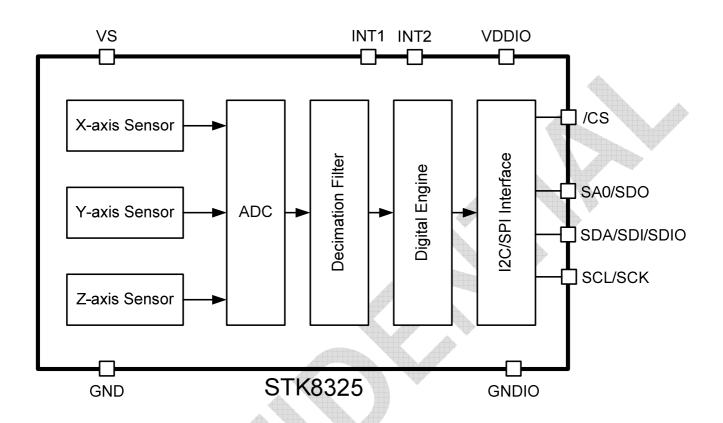
### Direction denotation

0	Output	GND	Ground
	Input	В	Bi-direction
PWR	Power	NC	Not Connected





# 3. FUNCTION BLOCK





# 4. ELECTRICAL SPECIFICATIONS

 $T_A = 25$ °C, VS = 2.6 V, VDDIO = 2.6 V, acceleration = 0 g,  $C_S = C_{VO} = 10 \,\mu\text{F}$  and 0.1  $\mu\text{F}$ 

Parameter	Test Conditions	Min	Тур	Max	Unit
POWER SUPPLY					
Operating Voltage Range (VS)		1.7	1.8	3.6	V
Interface Voltage Range (VDDIO)		1.62	1.8	3.6	V
Current consumption in normal mode			110		μΑ
Current consumption in suspend mode			1		μΑ
Current consumption in low-power mode	Sleep duration=25 ms Bandwidth=1k Hz		7		uA
Digital high level input voltage (VIH)		0.7 x VDDIO			V
Digital low level input voltage (VIL)				0.3 x VDDIO	V
High level output voltage (VOH) <sup>1</sup>		0.8 x VDDIO	·		V
Low level output voltage (VOL) <sup>1</sup>			>	0.2 x VDDIO	V
OUTPUT DATA RATE AND BANDWIDTH	Each axis				
Bandwidth (BW)			7.81		Hz
		<b></b>	15.63		Hz
			31.25		Hz
			62.5		Hz
			125		Hz
			250		Hz
			500		Hz
			1000		Hz
Output data rate (ODR) in normal mode			BW * 2		Hz

<sup>1.</sup> IOL = 10mA, IOH = -4mA



# 5. MECHANICAL SPECIFICATIONS

 $T_A = 25$ °C, VS = 2.6 V, VDDIO = 2.6 V, acceleration = 0 g,  $C_S = C_{I/O} = 10$   $\mu F$  and 0.1  $\mu F$ 

Parameter	Test Conditions	Min	Typical	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8		g
Non-linearity	Percentage of full scale		±0.5		%FS
Cross-Axis Sensitivity			1		%
OUTPUT RESOLUTION	Each axis		440		
±2 g Range	Full resolution		12	A	Bits
±4 g Range	Full resolution	<u> </u>	12		Bits
±8 g Range	Full resolution		12		Bits
SENSITIVITY	Each axis	44			
	±2g, 12-bit resolution		1024		LSB/g
Sensitivity at XOUT, YOUT, ZOUT	±4g, 12-bit resolution		512		LSB/g
	±8g, 12-bit resolution		256		LSB/g
Sensitivity Change Due to Temperature	X-, Y-, Z-Axes		±0.02		%/°C
0 g OFFSET <sup>1</sup>	Each axis				
0 g Output for XOUT, YOUT, ZOUT		<b>.</b>	±50		mg
0 g Offset Change Due to Temperature	X-, Y-, Z-Axes		±1		mg/°C
NOISE					
X-, Y-, Z-Axes	±2g, 12-bit resolution BW = 62.5 Hz		200		μg/sqrt(Hz)

<sup>1.</sup> These parameters are tested in production at final test, and could slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.



### 6. ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings	Maximum value	Unit
VS	Supply voltage	-0.3 to 3.6	V
VDDIO	Digital Interface Supply Voltage	-0.3 to 3.6	V
Vin	Input voltage on any control pin	-0.3 to 3.6	V
Aunp	Acceleration (any axis, unpowered)	10000	g
Тор	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-40 to +125	°C
	<u> </u>	2 (HBM)	kV
ESD	Electrostatic dischange and estima	500 (CDM)	V
	Electrostatic discharge protection	200 (MM)	V
		100 (Latch Up)	mA

### 7. DIGITAL INTERFACE

Both  $I^2C$  and SPI digital interface are available in STK8325. In both cases, the STK8325 operates as a slave device. /CS (chip select) pin state is used to select the operation interface. The  $I^2C$  mode is enabled if the /CS pin is tied high to VDDIO. And the SPI mode is enabled when the /CS pin is tied to low.

#### 7.1 **|2C**

All registers in STK8325 can be accessed via the  $I^2C$  bus. All operations can be controlled by the related registers. There are two signals associated with the  $I^2C$  bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional signal used for sending and receiving the data to/from the interface. Both signals are pull-up to  $V_{DD\ I/O}$  through an external resistor.

The Slave Address associated to the STK8325 is 0x0F or 0x1F which is modified by the ADDSEL pin. If the ADDSEL pin is connected to the VDDIO, the address is 0x1F, otherwise if the ADDSEL pin is connected to ground, the address is 0x0F. This solution permits to connect and address two different accelerometers to the same I<sup>2</sup>C lines.

A watchdog timer (WDT) is used to prevent the I<sup>2</sup>C bus lock-up by STK8325. The I<sup>2</sup>C bus will be reset and return to normal operation state once the WDT is reached. The WDT can be enabled/disabled by I2C\_WDT\_EN bit and the timer period can be set by I2C\_WDT\_SEL bit in register INTFCFG(0x34)

The STK8325 I<sup>2</sup>C command format description for reading and writing operation between the host and STK8325 are shown in the following timing chart.

#### **Slave Address**

/CS pin	SA0 pin	Slave Address (7-bit)	R/W Command Bit	OPERATION
		0x1F	0	Write Data to STK8325
1 or float		UXIF	1	Read Data form STK8325
	0	0x0F	0	Write Data to STK8325
			1	Read Data form STK8325

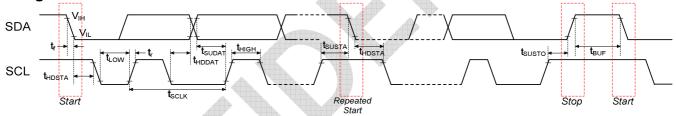


Characteristics of the I<sup>2</sup>C Timing

0	Parameter	Standa	rd Mode	Fast Mode		1124
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
fsclk	SCL clock frequency	10	100	10	400	kHz
<b>t</b> HDSTA	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	_	0.6	_	μs
t <sub>LOW</sub>	LOW period of the SCL clock	4.7	_	1.3	_	μs
tніgн	HIGH period of the SCL clock	4.0	_	0.6		μs
<b>t</b> susta	Set-up time for a repeated START condition	4.7	_	0.6	44	μs
thddat	Data hold time	0	_	0		ns
tsudat	Data set-up time	250	_	100		ns
tr	Rise time of both SDA and SCL signals	_	1000	D-4	300	ns
t <sub>f</sub>	Fall time of both SDA and SCL signals	- 4	300		300	ns
tsusto	Set-up time for STOP condition	4.0	_	0.6	_	μs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7		1.3	_	μs

Note: f<sub>SCLK</sub> is the (t<sub>SCLK</sub>)-1.

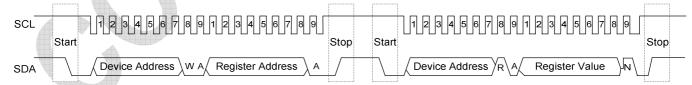
#### Timing Chart of the I<sup>2</sup>C



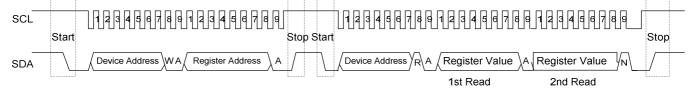
#### I<sup>2</sup>C Write Command



#### I<sup>2</sup>C Read Data



### I<sup>2</sup>C Sequential Read Data

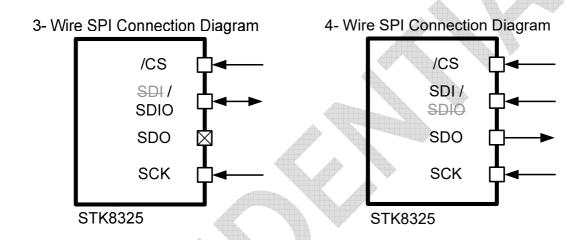




### 7.2 **SPI**

For SPI, either 3- or 4-wire configuration is possible. The STK8325 is also compatible with '00' (mode 0) and '11' (mode 3) SPI mode. The automatic selection between '00' [CPOL = 0 and CPHA = 0] and '11' [CPOL = 1 and CPHA = 1] is done based on the SCK value at the falling edge of /CS.

The 3-or 4-wire SPI connection diagram are shown below. The maximum SPI clock speed is 8MHz with 25pF maximum loading. The 3-wire SPI can be selected by setting SPI\_3WM bit in INTFCFG (0x34) to 1. When using 3-wire SPI, it is recommended that the SDO pin either be pulled up to VDDIO or be pulled down to GND via a 10 k $\Omega$  resistor.

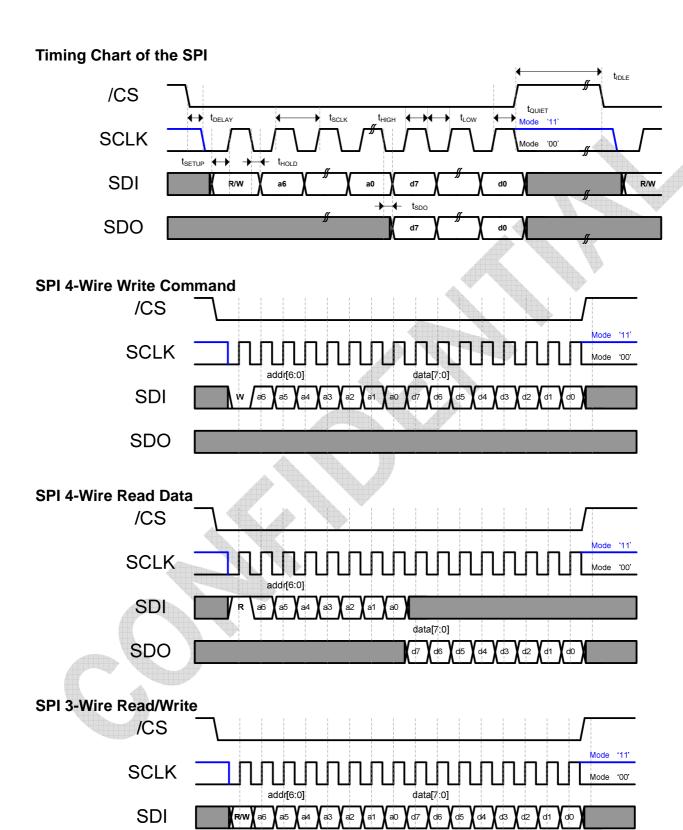


The timing diagram for 3-wire and 4-wire SPI reads or writes is shown in the following figure.

#### Characteristics of the SPI Timing

Symbol	Parameter	Min.	Max.	Unit
f <sub>SCLK</sub>	SPI clock frequency.		8	MHz
tsclk	1/ fsclk	12.5	_	ns
t <sub>HIGH</sub>	SCLK high pulse width.	6.25		ns
t <sub>LOW</sub>	SCLK low pulse width.	6.25		ns
tDELAY	/CS falling edge to SCLK falling edge.	30	_	ns
tQUITE	SCLK rising edge to /CS rising edge	70	_	ns
tsetup	Set-up time for SDI	20	_	ns
thold	Hold time for SDI	20	_	ns
t <sub>SDO</sub>	SDO output delay.	_	20	ns
tidle	SPI bus idle time between two success bus transactions.	20	_	ns







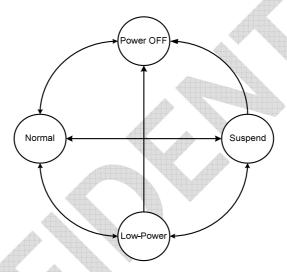
### 8. PRINPICLE OF OPERATION

### 8.1 Mode of Operation

STK8325 acts as a slave and can communicate with a master (uC or uP). Acceleration data and status information can be accessed with I<sup>2</sup>C or SPI interface. The interrupt pin are freely configured by user, depends on different requirements.

### 8.2 Power Management

STK8325 has three different power modes, Normal Mode, Low-Power Mode and Suspend Mode. After power-on, it will enter Normal Mode, and user can transfer to Low-Power Mode or Suspend Mode for power-saving purpose.



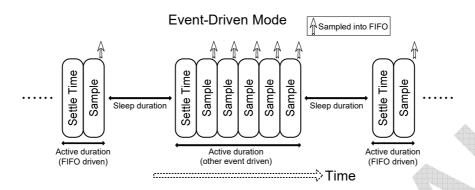
In Normal Mode, all functions are available and data acquisition is performed continuously.

In **Suspend Mode**, whole analog and oscillator are power-down. No data acquisition is performed. Only register reading and writing to SUSPEND bit in register <u>POWMODE</u> (0x11) or register <u>SWRST</u> (0x14) are supported. Suspend mode can be entered by set SUSPEND bit in register <u>POWMODE</u> (0x11) to 1. In the suspend mode, the output data doesn't clear or update, but keeps the last value before entering into suspend mode.

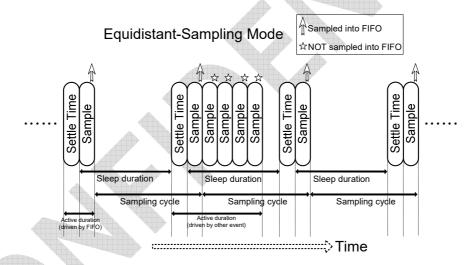
In **Low-Power Mode**, STK8325 will switch between wake-up and sleep phase. In wake-up phase, the device is full functional operation, just like in Normal Mode. In sleep phase, the analog circuit is power-down except oscillator. Average current consumption can be effectively reduced by entering low-power mode. Low-power mode can be entered by setting LOWPOWER bit in register <u>POWMODE</u> (0x11) to 1.

Two kinds timing behaviors of low-power mode, event-driven mode (EDM) and equidistant-sampling mode (ESM), it can be selected by SLEEP\_TIMER bit in register <a href="POWMODE">POWMODE</a> (0x11). When SLEEP\_TIMER is set to '0', the event-driven mode (EDM) is selected. In EDM,,the duration of the wake-up phase depends on the number of samples required by the enabled interrupt engines. If an interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary interrupt), or until the interrupt is reset (latched interrupt). If no interrupt is detected, the device enters the sleep phase immediately after the required number of acceleration samples have been taken and an active interface access cycle has ended. The EDM mode is recommended for power-critical applications which do not use the FIFO. The figure below shows the timing diagram for low-power modes when EDM is selected.





When SLEEP\_TIMER is set to '1', the equidistant-sampling mode (ESM) is selected. The ESM is recommended when the FIFO is used since it ensures that equidistant samples are sampled into the FIFO regardless of whether the active phase is extended by active interrupt engines or interface activity. In ESM, the sleep duration is defined as shown in following figure. The FIFO sampling cycle is the sum of the sleep duration and the sensor settling time. Since interrupt engines can extend the active phase to exceed the sleep duration, equidistant sampling is only guaranteed if the bandwidth has been chosen such that 1/(2 \* bandwidth) = n \* (sleep duration) where n is an integer. If this condition is infringed, equidistant sampling is not possible. Once the sleep time has elapsed the device will store the next available sample in the FIFO. This set-up condition is not recommended as it may result in timing jitter.



The duration of sleep phase can be set by SLEEP\_DUR [3:0] in register POWMODE (0x11).

TO VICE THE PARTY OF THE PARTY		
SLEEP_DUR[3:0]	Duration (ms)	Actually ODR with 1kHz bandwidth (Hz)
4'b0000 ~ 4'b0101	0.5	295
4'b0110	1	255
4'b0111	2	202
4'b1000	4	140
4'b1001	6	110
4'b1010	10	75
4'b1011	25	34
4'b1100	50	18
4'b1101	100	10
4'b1110	500	2
4'b1111	1000	1



### 8.3 Data, Range and Bandwidth

#### **Acceleration Data**

The acceleration data of STK8325 is 12 bits and is given in two's complement format. The MSB in each axis will be stored in register XOUT2/YOUT2/ZOUT2 (0x03, 0x05, 0x07) individually, and the LSB will be stored in register XOUT1/YOUT1/ZOUT1 (0x02, 0x04, 0x06) individually. The NEW\_X/NEW\_Y/NEW\_Z bit in register XOUT1/YOUT1/ZOUT1 (0x02, 0x04, 0x06) is used for new data flag, and it will be set to 1 if the data is updated, and reset if either the corresponding MSB or LSB is read. Reading the acceleration data registers shall always start with the LSB part due to the data protection function. When data protection function is enabled, the content of an MSB register will be updated by reading the corresponding LSB register. The data protection function can be disabled (enabled) by writing '1' ('0') to the PROTECT\_DIS bit in register DATASETUP (0x13). With disabled data protection, the content of both MSB and LSB registers is updated by a new value immediately.

#### Range

The STK8325 supports four different acceleration measurement ranges. A measurement range can be selected by RANGE[3:0] bits in register RANGESEL (0x0F).

			Total Control of the
RANG	GE[3:0]	Sensing Range	Resolution
4'b0011	0x3	±2g	0.98 mg/LSB
4'b0101	0x5	±4g	1.95 mg/LSB
4'b1000	0x8	±8g	3.91 mg/LSB
otl	ners	undefined	undefined

#### **Bandwidth**

There are two different data stream of STK8325, unfiltered data and filtered data. Unfiltered data is sampled as 2 kHz, and the sample rate of filtered data depends on the selected bandwidth; it is twice of the bandwidth. If the DATA\_SEL bit in register <a href="DATASETUP">DATASETUP</a> (0x13) is set to '0' ('1'), the filtered (unfiltered) data will be stored in the XOUT/YOUT/ZOUT data register. Each of the data stream can be separately offset-compensated, and also can be the data source of interrupts controller. The actual bandwidth for the filtered data can be selected by BW [4:0] bits in register <a href="BWSEL">BWSEL</a> (0x10).

BW[4:0]	Actual Bandwidth (Hz)
5'b00xxx	7.81
5'b01000	7.81
5'b01001	15.63
5'b01010	31.25
5'b01011	62.5
5'b01100	125
5'b01101	250
5'b01110	500
5'b01111	1000
5'b1xxxx	1000

# 8.4 Motion Algorithm Status and Interrupt Event Detection

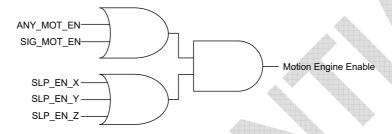
The following table shows the interrupt events offered by STK8325. Several interrupt engines and two INT pins are integrated for conveniently motion detection. Each interrupt could be enabled independently, and mapped into any of two INT pins. If the condition of enabled interrupt is fulfilled, the corresponding status is set to '1' and selected INT pin is asserted. The INT pin state is logical 'or' combination of all mapped interrupts. The INT pin state is logical 'or' combination of all mapped interrupts. If an interrupt is disabled, all active pins and status are reset immediately.



Two motion algorithms, any-motion and significant motion, used for detecting user movement can flexibly choose three independent axes as the data source via register <a href="INTEN1">INTEN1</a> (0x16), and the event signal is triggered by an "OR" combination of the enabled axes.

Interrupt Event	Control Bit	Status Bit in Register INTSTS1/2 (0x09, 0x0A)
New Data	DATA_EN in <u>INTEN2</u> (0x17)	DATA_STS
	SLP_EN_Z in INTEN1 (0x16)	SLP_1ST_Z
Any Motion (Clans)	SLP_EN_Y in <u>INTEN1</u> (0x16)	SLP_1ST_Y
Any-Motion (Slope) Significant Motion	SLP_EN_X in INTEN1 (0x16)	SLP_1ST_X
Significant Motion	ANY_MOT_EN in SIGMOT2 (0x2A)	ANY_MOT_STS
	SIG_MOT_EN in SIGMOT2 (0x2A)	SIG_MOT_STS

Note: Motion algorithm engine follows the logic shown below.



#### **Interrupt Latch Mode**

There are three different interrupt latch modes of Any-Motion (Slope) and Significant Motion: non-latched, temporary, and latched. The modes can be selected by the INT\_LATCH [3:0] bits in register <a href="INTCFG2">INTCFG2</a> (0x21). The following table shows the different configurations of interrupt modes in INT\_LATCH [3:0].

INT_LATCH[3:0]	Output Mode		
4'b0000	non-latched		
4'b0001	temporary, 250ms		
4'b0010	temporary, 500ms		
4'b0011	temporary, 1s		
4'b0100	temporary, 2s		
4'b0101	temporary, 4s		
4'b0110	temporary, 8s		
4'b0111	latched		
4'b1000	non-latched		
4'b1001	temporary, 250us		
4'b1010	temporary, 500us		
4'b1011	temporary, 1ms		
4'b1100	temporary, 12.5ms		
4'b1101	temporary, 25ms		
4'b1110	temporary, 50ms		
4'b1111	latched		

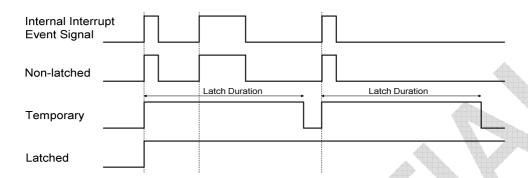
In the **non-latched mode**, the corresponding status and mapped INT pin are clear as soon as the activation condition is no more valid.

In the **latched mode**, the status and mapped INT pins are cleared only by setting '1' to the INT\_RST bit in register INTCFG2 (0x21). If the activation condition still holds when it is cleared, the interrupt pin and status will be both asserted again.

In the **temporary mode**, an asserted interrupt and selected pin are cleared after a defined period of time. The following figure shows the behavior of three interrupt modes.



Both filtered and unfiltered data could be the data source of the interrupt events. Setting the corresponding bit in register <u>DATASETUP</u> (0x13) to '0'('1') will select the filtered(unfiltered) data as the data source for interrupt events.



Interrupt latch mode control bits only apply to Any-Motion (Slope) and Significant Motion. Other interrupt events are fixed to their own latch mode which are shown in the following table.

		Almente Ver	
Interrupt Event	Туре	Latch mode	Clear
New data	Status	Non-latch	Auto clear after data update
Any-Motion (Slope)	Programmable	Programmable	Based on configuration
Significant Motion	Programmable	Programmable	Based on configuration
FIFO Watermark	Status	Non-latch	After the event is invalid
FIFO Full	Status	Non-latch	After the event is invalid

#### **Interrupt Pin Mapping and Output Types**

The mapping of interrupts to the INT1 or INT2 is controlled by registers <a href="INTMAP2">INTMAP2</a> (0x1A). Setting the corresponding bit to '1'('0') maps(un-maps) the related interrupt to the INT pins.

Both INT1 and INT2 can be configured in register <u>INTCFG1</u> (0x20). The output and active level can be set as Push-Pull/Open-Drain and as active-high/active-low.



### 8.5 Offset Compensation

#### **Manual Compensation**

STK8325 offers the manual digital offset-compensation method. It is done by adding a compensation value to the acceleration data coming from the ADC. The registers OFSTX/Y/Z (0x38, 0x39, 0x3A) are used to for the offset compensation purpose and are given in two's complement format. 1 LSB of OFSTX/Y/Z represents 7.81mg in any sensing range. By writing '1' to the OFST\_RST bit in register OFSTCOMP1 (0x36), all offset compensation registers are reset to zero.

It is recommended to write into these registers immediately after a new data interrupt in order not to disturb running offset computations.

### 8.6 **FIFO**

#### **FIFO Operating Modes**

The STK8325 features an integrated FIFO memory capable of storing up to 32 frames, which allows collecting 32 samples of 12 bits for the x, y and z- axis data at the same point on the timeline or storing 96 samples of 12 bits for the single axis data.

FIFO use allows consistent power saving for the system, it can wake up only when needed and burst the data out from the FIFO. The FIFO buffer can work according to five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream and Stream-to-FIFO mode.

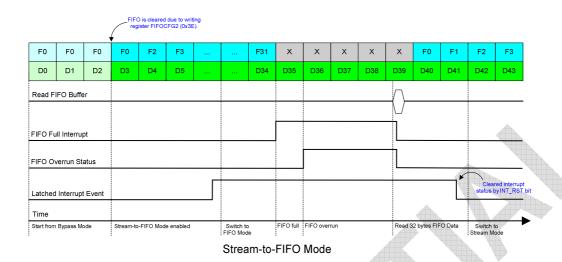
In **Bypass mode**, only the current sensor data can be read out from the FIFO address. Essentially, the FIFO behaves like the Stream mode with a depth of 1. If user reads the acceleration data from FIFO data register, it can be guaranteed that the x, y, and z- axis data are from the same timestamp. To avoid mixing of data from different axes occur while the data registers are updated sequentially. When new data arrives, the old data will be overwritten and the overrun bit is set to '1'.

In **FIFO mode**, the acceleration data of the selected axes are continuously stored in the buffer until the unread data reaches 32 frames for x, y, z- axis or 96 frames for the single axis. When the FIFO is full, the data collection is stopped and new data is ignored. If FIFO mode is enabled, a watermark interrupt will be triggered when the buffer is filled to a configurable level. Once the buffer is full, a FIFO-full interrupt also generates if it has been enabled.

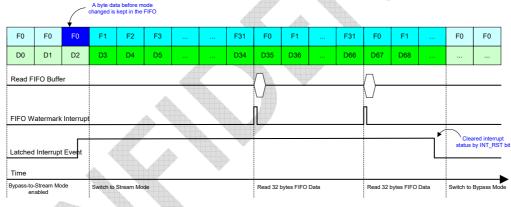
In **Stream mode**, the acceleration data of the selected axes are continuously updated in the buffer. When the buffer is full, as new data arrives the oldest data is discarded and overwritten by the newer. If an overrun occurs, the FIFO overrun flag is asserted. If Stream mode enabled, a watermark interrupt is triggered when the buffer is filled to a configurable level. Once the buffer is full, a FIFO-full interrupt generates if it has been enabled.

In **Stream-to-FIFO mode**, the FIFO buffer starts operating in Stream mode and switches to FIFO mode when the Any-Motion (slope) or Significant Motion interrupt occurs. User must be sure that the interrupt is configured to latched mode. When the FIFO is full, data collecting is stopped. This mode can be used for analyzing the samples history which recorded before the interrupt event. The recommendation operation is to read FIFO content after FIFO mode is triggered and FIFO buffer is full and stopped capturing data.





In **Bypass-to-Stream mode**, the FIFO buffer starts in Bypass mode and switches to Stream mode when the Any-Motion (slope) or Significant Motion interrupt occurs. User must be sure that interrupt is configured to the latched mode. This mode can be used for analyzing the samples after event occurred. In this mode, user is recommended to enable watermark interrupt to avoid loss of data.



Bypass-to-Stream Mode

Note: When the requested event takes place, the FIFO mode change is triggered if and only if the event flag is routed to the INT1 in Stream-to-FIFO mode and Bypass-to-Stream mode.

The FIFO operation can be controlled by register <u>FIFOCFG2</u> (0x3E) FIFO\_MODE[2:0], and the corresponding settings are shown in the table below.

FIFO_MODE[2:0]	Mode selection
3'b000	Bypass mode
3'b001	FIFO mode
3'b010	reserved
3'b011	Stream-to-FIFO mode
3'b100	Bypass-to-Stream mode
3'b101	reserved
3'b110	Stream mode
3'b111	reserved

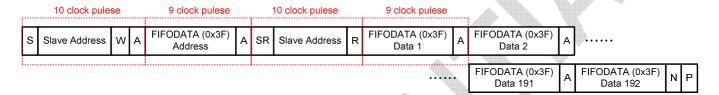


The FIFO content, full interrupt, and watermark interrupt will be cleared and reset when writing to register <u>FIFOCFG1</u> (0x3D) or register <u>FIFOCFG2</u> (0x3E).

#### **FIFO Data Readout**

The latest frame stored in FIFO is identical to the acceleration data in the read-out registers (0x02) to (0x07). Thus, all configuration settings apply to the FIFO frame as well as the acceleration data readout registers. The readout can be performed using burst mode since the read address counter is no longer incremented, when the burst read access starts below address <u>FIFODATA</u> (0x3F). A single burst is recommended to read out one or more frames at a time.

The I2C needs about 29 clock pulses to start communication plus an additional 9 clock pulses for every byte to read. So, in the case of I2C standard mode being used (100 kHz), total 32 frames XYZ-axes FIFO data reading takes (29 + 9 \* 32 \* 6) clock pulses, about 17.57 ms. In another case of I2C fast mode being used (400 kHz), it takes about 4.39 ms.



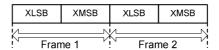
Register FIFOCFG2 (0x3E) FIFO\_DATA\_SEL[1:0] controls the acceleration data of which axes are stored in the FIFO. The depth of the FIFO depends on whether all or a single axis is selected. Moreover, FIFO\_INTERVAL[1:0] controls the acceleration data storage interval, and users can select the subsampling frequency in every one, two, four, or eight samples that the acceleration data will be automatically stored into FIFO. The buffer content, FIFO full interrupt and watermark interrupt are cleared and reset if user write to the register FIFOCFG1 (0x3D) or FIFOCFG2 (0x3E).

FIFO_DATA_SEL [1:0]	FIFO data source
2'b00	XYZ-axes
2'b01	X-axis only
2'b10	Y-axis only
2'b11	Z-axis only

If all axes are enabled, the format of the data read-out from register FIFODATA (0x3F) is as follows:

XLSB	XMSB	YLSB	YMSB	ZLSB	ZMSB
1/					
		Fran	me 1		

If only one axis is enabled, the format of the data read-out from register <u>FIFODATA</u> (0x3F) is as follows: (Example shown x-axis only, other axes are equivalent).



To be sure the data integrity, a frame shall be the minimum unit for FIFO reading. If a frame is not properly read due to an incomplete read operation, the remaining part of the frame is discarded.

If user read out a length of frame data which is beyond the FIFO fill level, zeroes (0, 0, 0) will be presented.



#### FIFO Frame Counter and Overrun Flag

Register <u>FIFOSTS</u> (0x0C) FIFO\_FRAME\_CNT[6:0] indicates the current frame level of the buffer. The FIFO\_OVR bit will be set as '1' if a new frame arrives but the FIFO is full. Once the frames are read out and FIFO\_FRAME\_CNT[6:0] is decremented, the FIFO\_OVR bit will be reset to '0'.

The FIFO buffer, FIFO\_FRAME\_CNT[6:0], and FIFO\_OVR bit are all reset when user writes to <u>FIFOCFG1</u> (0x3D) or <u>FIFOCFG2</u> (0x3E).

#### **FIFO Interrupts**

The FIFO controller can generate two different interrupt events, a FIFO-full and a watermark event. The FIFO-full and watermark interrupts are both available in all FIFO operating modes.

In order to enable the watermark interrupt, the register <u>INTEN2</u> (0x17) FWM\_EN bit and register <u>INTMAP2</u> (0x1A) FWM2INT1 or FWM2INT2 bit must be set to '1' that routes the interrupt signal to INT1 or INT2 pins.

The watermark interrupt is asserted when the frames level in the buffer reaches the level defined by register <a href="FIFOCFG1">FIFO\_WM\_LV</a>. Meanwhile, the status of the watermark interrupt can be read back via register <a href="INTSTS2">INTSTS2</a> (0x0A) FWM\_STS bit.

In order to enable the FIFO-full interrupt, register <a href="INTEN2">INTEN2</a> (0x17) FFULL\_EN bit as well as register <a href="INTMAP2">INTMAP2</a> (0x1A) FFULL2INT1 or FFULL2INT2 bit must also be set to '1'. The FIFO-full interrupt is triggered when the buffer has been fully occupied and that means 32 frames in FIFO mode, 32 frames in Stream mode, and 1 frame in Bypass mode. The status of the FIFO-full interrupt is also shown in register <a href="INTSTS2">INTSTS2</a> (0x0A) FFULL\_STS bit.

The interrupts and status of FIFO-full and watermark will both be reset after writing to register <u>FIFOCFG1</u> (0x3D) or <u>FIFOCFG2</u> (0x3E) and the FIFO buffer is also simultaneously cleared.



# 9. REGISTER DEFINATION

# 9.1 Register Map

ADDR	REG NAME				В	IT				Default
	_	7	6	5	4	3	2	1	0	
00h	CHIP_ID					ID[7:0]		4		25h
01h	RESERVED				rese	rved				00h
02h	XOUT1		XOU	T[3:0]			rese	erved		00h
03h	XOUT2		XOUT[11:4]							00h
04h	YOUT1		YOU	T[3:0]			rese	erved		00h
05h	YOUT2				YOUT	[11:4]				00h
06h	ZOUT1		ZOU	T[3:0]			rese	erved		00h
07h	ZOUT2				ZOUT			- AP V		00h
08h	RESERVED		reserved							00h
09h	INTSTS1			reserved			ANY_MOT_STS	reserved	SIG_MOT_STS	00h
0Ah	INTSTS2	DATA_STS	FWM_STS	FFULL_STS		· .	reserved	1		00h
0Bh	EVENTINFO1	reserved	SLPSIGN_Z	SLPSIGN_Y	SLPSIGN_X	reserved	SLP_1ST_Z	SLP_1ST_Y	SLP_1ST_X	00h
0Ch	<u>FIFOSTS</u>	FIFO_OVR				_FRAME_CN	T[6:0]			00h
0D-0Eh	RESERVED				rese	rved				00h
0Fh	RANGESEL		rese	rved				SE[3:0]		03h
10h	BWSEL		reserved	Alesey			BW[4:0]			1Fh
11h	POWMODE	SUSPEND	LOWPOWER	SLEEP_TIMER	411	SLEEP_	DUR[3:0]		reserved	00h
12h	RESERVED			1	rese	rved				00h
13h	DATASETUP	DATA_SEL	PROTECT_DIS				erved			00h
14h	SWRST			4	SWRS	ST[7:0]				00h
15h	RESERVED				rese	rved	<u> </u>	I		00h
16h	INTEN1		4110	reserved			SLP_EN_Z	SLP_EN_Y	SLP_EN_X	00h
17h	INTEN2	reserved	FWM_EN	FFULL_EN	DATA_EN		rese	erved		00h
18h	RESERVED				rese	rved				00h
19h	INTMAP1	SIGMOT2INT2	reserved	ANYMOT2INT2		rved	ANYMOT2INT1	reserved	SIGMOT2INT1	00h
1Ah	INTMAP2	DATA2INT2	FWM2INT2	FFULL2INT2	rese	rved	FFULL2INT1	FWM2INT1	DATA2INT1	00h
1Bh-1Fh	RESERVED				rese	rved	T	T		00h
20h	INTCFG1		rese	rved		INT2_OD	INT2_LV	INT1_OD	INT1_LV	05h
21h	INTCFG2	INT_RST		reserved			INT_LA	TCH[3:0]		00h
22h-26h	RESERVED					rved		T		00h
27h	SLOPEDLY			rese	rved			SLP_D	UR[1:0]	00h
28h	SLOPETHD				SLP_T	HD[7:0]				14h
29h	SIGMOT1				SKIP_T	IME[7:0]	1	1		96h
2Ah	SIGMOT2		reserved ANY_MOT_EN SIG_MOT_EN SKIP_TIME[8]							02h
2Bh	SIGMOT3	reserved			PF	ROOF_TIME[6	S:0]			32h
2Ch-32h	RESERVED					rved				00h
33h	<u>PRIMIF</u>				SPI_PRIN	//ARY[7:0]	1	1		00h
34h	INTFCFG			reserved			I2C_WDT_EN	I2C_WDT_SEL	SPI_3WM	00h
35h	RESERVED				rese	rved				00h



36h	OFSTCOMP1	OFST_RST			reserved		00h	
37h	RESERVED		reserved					
38h	<u>OFSTX</u>			OFST_	_X[7:0]		00h	
39h	<u>OFSTY</u>			OFST_	_Y[7:0]		00h	
3Ah	<u>OFSTZ</u>			OFST_	_Z[7:0]		00h	
3Bh-3Ch	RESERVED			rese	rved		00h	
3Dh	FIFOCFG1	reserved		FIF	FO_WM_LV[6:0]		00h	
3Eh	FIFOCFG2	FI	FO_MODE[2:0]	D_MODE[2:0] reserved FIFO_INTERVAL[1:0] FIFO_DATA_SEL[1:0]				
3Fh	<u>FIFODATA</u>			FIFOOI	UT[7:0]		00h	

# 9.2 Register Description

**CHIP\_ID** Register (00h)

	<del> </del>				410101010101	A 10	SISTORY CITY	
b7	b6	b5	b4	b3		b2	b1	b0
			CHIP_	ID[7:0]				
			8'b001	00101				
			R	0				

The register contains the chip identification code.

XOUT1 Register (02h)

b7	b6	b5	b4	b3		b2	b1	b0
	XOU <sup>*</sup>	T[3:0]			reserved			
	4'b(	0000		4'b0000				
		RO					RO	

XOUT1/XOUT2 register contain the x-axis acceleration data.

XOUT2 Register (03h)

	9		TOTAL TOTAL ACTIV				
b7	b6	b5	b4	b3	b2	b1	b0
		4	XOUT[1	1:4]			
		, 40	8'b00000	0000			
			RO				

YOUT1 Register (04h)

	9.010. (0.11)							
b7	b6	b5	b4	b3	b2	b1	b0	
	YOUT	Γ[3:0]		reserved				
	4'b0	000			4'b0	000		
	R	0			R			

YOUT1/YOUT2 register contain the y-axis acceleration data.

YOUT2 Register (05h)

Tallian Co.	310101 (0011)									
b7	b6	b5	b4	b3	b2	b1	b0			
		YOUT[11:4]								
	8'b00000000									
			R	0						

**ZOUT1** Register (06h)

b7	b6	b5	b4	b3	b2	b1	b0	
ZOUT[3:0]			reserved					
	4'b0000				4'b0000			
RO				R	0			

ZOUT1/ZOUT2 register contain the z-axis acceleration data.



**ZOUT2** Register (07h)

b7	b6	b5	b4	b3	b2	b1	b0
ZOUT[11:4]							
	8'b00000000						
	RO						

**INTSTS1** Register (09h)

_		<u> </u>						
	b7	b6	b5	b4	b3	b2	b1	b0
	reserved					ANY_MOT_STS	reserved	SIG_MOT_STS
	5'b00000				0	0	0	
	RO					RO	RO	RO

This register contains the interrupts status in STK8325.

BIT	BIT NAME	Description
0	SIG_MOT_STS	Significant motion interrupt status. '1': event triggered, '0': no event.
2	ANY_MOT_STS	Any-motion (slope) detection interrupt status. '1': event triggered, '0': no event.

**INTSTS2** Register (0Ah)

b7	b6	b5	b4	b3	b2		b1	b0
DATA_STS	FWM_STS	FFULL_STS			reserv	ed		
0	0	0			5'b000	00		
RO	RO	RO			RO			

This register contains the new data interrupt status in STK8325.

BIT	BIT NAME	Description
5	FFULL_STS	FIFO full interrupt status. '1': event triggered, '0': no event.
6	FWM_STS	FIFO watermark interrupt status. '1': event triggered, '0': no event.
7	DATA_STS	New data interrupt status. '1' : event triggered, '0' : no event.

EVENTINFO1 Register (0Bh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved	SLPSIGN_Z	SLPSIGN_Y	SLPSIGN_X	reserved	SLP_1ST_Z	SLP_1ST_Y	SLP_1ST_X
0	0	0	0	0	0	0	0
RO	RO	RO	RO	RO	RO	RO	RO

This register contains any-motion (slope) detection information.

BIT	BIT NAME	Description
0	SLP_1ST_X	1 : Motion on the X-axis cause SLOPE interrupt asserted.
1	SLP_1ST_Y	1 : Motion on the Y-axis cause SLOPE interrupt asserted.
2	SLP_1ST_Z	1 : Motion on the Z-axis cause SLOPE interrupt asserted.
4	SLPSIGN_X	Sign of acceleration slope on the X-axis that triggered the SLOPE interrupt.  0: positive. 1: negative.
5	SLPSIGN_Y	Sign of acceleration slope on the Y-axis that triggered the SLOPE interrupt.  0: positive. 1: negative.
6	SLPSIGN_Z	Sign of acceleration slope on the Z-axis that triggered the SLOPE interrupt.  0: positive. 1: negative.



FIFOSTS Register (0Ch)

b7	b6	b5	b4	b3	b2	b1	b0
FIFO_OVR	FIFO_FRAME_CNT[6:0]						
0		7'b0000000					
RO		RO					

This register contains FIFO status flags.

BIT	BIT NAME	Description
7	FIFO_OVR	FIFO overrun flag. '1': event triggered, '0': no event. Flag can be cleared by reading data from FIFODATA[7:0].
[6:0]	FIFO_FRAME_CNT[6:0]	Current fill level of FIFO buffer, it shows the number of unread frames stored in FIFO.

**RANGESEL** Register (0Fh)

b7	b6	b5	b4	b3	b2	b1	b0	
reserved				RANGE[3:0]				
	4'b0000			4'b0011				
RO				R	W			

This register contains the acceleration sensing range. It is recommended that set the suspend mode before changing the register RANGESEL(0x0F) to ensure correct output data.

RANG	E[3:0]	Sensing Range
4'b0011	0x3	±2g
4'b0101	0x5	±4g
4'b1000	0x8	±8g
oth	ers	undefined

**BWSEL** Register (10h)

b7	b6	b5	b4	A	b3	b2	b1	b0
	reserved					BW[4:0]		
	3'b000					5'b11111		
	RO					R/W		

This register contains the output data bandwidth selection. It is recommended that set the suspend mode before changing the register BWSEL(0x10) to ensure correct output data.

BW[4:0]	Actual Bandwidth (Hz)
5'b00xxx	7.81
5'b01000	7.81
5'b01001	15.63
5'b01010	31.25
5'b01011	62.5
5'b01100	125
5'b01101	250
5'b01110	500
5'b01111	1000
5'b1xxxx	1000

**POWMODE** Register (11h)

	Todoctody C							
b7	b6	b5	b4	b3	b2	b1	b0	
SUSPEND	LOWPOWER	SLEEP_TIMER		SLEEP_DUR[3:0]				
0	0	0		4'b0000				
R/W	R/W	R/W		R/W				

This register contains the power mode selection and the sleep time duration setting. It is recommended that set the suspend mode before changing the register POWMODE(0x11) to ensure correct output data.



BIT	BIT NAME		Descripti	on
		Sleep time duration.		
		SLEEP_DUR[3:0]	Duration (ms)	
		4'b0000 ~ 4'b0101	0.5	
		4'b0110	1	
		4'b0111	2	
		4'b1000	4	
[4:1]	SLEEP_DUR[3:0]	4'b1001	6	
' '		4'b1010	10	
		4'b1011	25	
		4'b1100	50	
		4'b1101	100	
		4'b1110	500	
		4'b1111	1000	
		Sleep timer control bit in	low-power mode.	
5	SLEEP_TIMER	0 : event-driven.	.е реже:е.е.	
	_	1 : equidistant sampling.		
6	LOWPOWER	0 : low-power mode disal		
0	LOWPOWER	1 : low-power mode enab		
7	SUSPEND	0 : suspend mode disable		
/	SUSPEND	1 : suspend mode enable		

**DATASETUP** Register (13h)

b7	b6	b5	b4	b:	3	b2	b1	b0
DATA_SEL	PROTECT_DIS				rese	erved		
0	0		6'b000000					
R/W	R/W		4		R	O		

This register is used to select if the output data is filtered or unfiltered and how the output data contained in the register XOUT1/XOUT2, YOUT1/YOUT2, ZOUT1/ZOUT2 are updated.

BIT	BIT NAME	Description
6	PROTECT_DIS	0 : Enable the data protection function.     1 : Disable the data protection function.
7	DATA_SEL	0 : Data output filtered. 1 : Data output unfiltered.

**SWRST** Register (14h)

b7	b6	b5		b4	b3	b2	b1	b0	
	SWRST[7:0]								
	8'b0000000								
	W								

This register is used to software reset. Write 0xB6 into SWRST to reset all the registers to default value.

#### **INTEN1** Register (16h)

b7	b6	b5	b4	b3	b2	b1	b0
	4	reserved			SLP_EN_Z	SLP_EN_Y	SLP_EN_X
		5'b00000			0	0	0
		RO			R/W	R/W	R/W

This register contains the several interrupt enable bit.

BIT	BIT NAME	Description
0	SLP_EN_X	0 : Disable X-axis any-motion (slope) interrupt.
U		1 : Enable X-axis any-motion (slope) interrupt.
4	SLP_EN_Y	0 : Disable Y-axis any-motion (slope) interrupt.
'		1 : Enable Y-axis any-motion (slope) interrupt.
2	CLD EN 7	0 : Disable Z-axis any-motion (slope) interrupt.
	SLP_EN_Z	1 : Enable Z-axis any-motion (slope) interrupt.



**INTEN2** Register (17h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved	FWM_EN	FFULL_EN	DATA_EN	reserved			
0	0	0	0	4'b0000			
RO	R/W	R/W	R/W	RO			

This register contains the several interrupt enable bit.

BIT	BIT NAME	Descri	iption
4	DATA_EN	0 : Disable new data interrupt.	
4	DATA_EN	1 : Enable new data interrupt.	
_	FFULL EN	0 : Disable FIFO full interrupt.	
5	FFULL_EIN	1 : Enable FIFO full interrupt.	
6	FWM EN	0 : Disable FIFO watermark interrupt.	
0	L A A I A I	1 : Enable FIFO watermark interrupt.	

**INTMAP1** Register (19h)

b7	b6	b5	b4	b3	b2	b1	b0
SIGMOT2INT2	reserved	ANYMOT2INT2	reserved		ANYMOT2INT1	reserved	SIGMOT2INT1
0	0	0	2'b00		0	0	0
R/W	RO	R/W	R	0	R/W	RO	R/W

This register is used to map the related interrupt to the desired INT pin.

BIT	BIT NAME	Description		
0	SIGMOT2INT1	0 : Do not map significant motion interrupt to INT1. 1 : Map significant motion interrupt to INT1.		
2 ANYMOT2INT1 0 : Do not map any-motion (slope) interrupt to INT1.  1 : Map any-motion (slope) interrupt to INT1.				
5	ANYMOT2INT2	0 : Do not map any-motion (slope) interrupt to INT2. 1 : Map any-motion (slope) interrupt to INT2.		
7	SIGMOT2INT2	0 : Do not map significant motion interrupt to INT2. 1 : Map significant motion interrupt to INT2.		

INTMAP2 Register (1Ah)

	<u> </u>	- Version Assistr	VIDEO"				
b7	b6	b5	b4	b3	b2	b1	b0
DATA2INT2	FWM2INT2	FFULL2INT2	reserved		FFULL2INT1	FWM2INT1	DATA2INT1
0	0	0	2'b00		0	0	0
R/W	R/W	R/W		.0	R/W	R/W	R/W

This register is used to map the related interrupt to the desired INT pin.

BIT	BIT NAME	Description
0	DATA2INT1	0 : Do not map new data interrupt to INT1. 1 : Map new data interrupt to INT1.
1	FWM2INT1	0 : Do not map FIFO watermark interrupt to INT1. 1 : Map FIFO watermark interrupt to INT1.
2	FFULL2INT1	0 : Do not map FIFO full interrupt to INT1. 1 : Map FIFO full interrupt to INT1.
5	FFULL2INT2	0 : Do not map new data interrupt to INT2. 1 : Map new data interrupt to INT2.
6	FWM2INT2	0 : Do not map FIFO watermark interrupt to INT2. 1 : Map FIFO watermark interrupt to INT2.
7	DATA2INT2	0 : Do not map FIFO full interrupt to INT2. 1 : Map FIFO full interrupt to INT2.



**INTCFG1** Register (20h)

b7	b6	b5	b4	b3	b2	b1	b0
	reserved				INT2_LV	INT1_OD	INT1_LV
	4'b0	0000		0	1	0	1
RO			R/W	R/W	R/W	R/W	

This register is used to define the INT1 and INT2 pins output type and active level. Open-drain or Push-pull output type and active high or active low can be selected.

BIT	BIT NAME		Description
0	INT1_LV	INT1 active level selection. 0 : Active low. 1 : Active high.	
1	INT1_OD	INT1 output type selection. 0 : Push-pull output type. 1 : Open-drain output type.	
2	INT2_LV	INT2 active level selection. 0 : Active low. 1 : Active high.	
3	INT2_OD	INT2 output type selection. 0 : Push-pull output type. 1 : Open-drain output type.	

**INTCFG2** Register (21h)

	- 3			ASSESSED VEISSED			
b7	b6	b5	b4	b3	b2	b1	b0
INT_RST		reserved			INT_LA	ГСН[3:0]	
0		3'b000			4'b0	0000	
R/W		RO			R/	W	

This register is used to reset latched interrupt pin and select the interrupt mode.

BIT	BIT NAME		Description						
		INT pin output mode sele	ction.						
		INT_LATCH[3:0]	Output Mode						
		4'b0000	non-latched						
		4'b0001	temporary, 250ms						
		4'b0010	temporary, 500ms						
		4'b0011	temporary, 1s						
		4'b0100	temporary, 2s						
		4'b0101	temporary, 4s						
[0.0]	INIT LATCHICAGO	4'b0110	temporary, 8s						
[3:0]	INT_LATCH[3:0]	4'b0111	latched						
		4'b1000	non-latched						
		4'b1001	temporary, 250us						
		4'b1010	temporary, 500us						
		4'b1011	temporary, 1ms						
444		4'b1100	temporary, 12.5ms						
		4'b1101	temporary, 25ms						
		4'b1110	temporary, 50ms						
		4'b1111	latched						
7	INT_RST	1 : Reset any latched inte	rrupt pin.						

**SLOPEDLY** Register (27h)

b7	b6	b5	b4	b3	b2	b1	b0
	reserved						
		6'b00	0000			2'b	000
RO						R/	W

This register is used to set the number of samples needed in slope detection. The actual number of samples will be equal to SLP\_DUR[1:0] + 1.



**SLOPETHD** Register (28h)

b7	b6	b5	b4	b3	b2	b1	b0
	SLP_THD[7:0]						
			8'b000	10100			
			R/	W			

This register is used to set the threshold value for the slope detection. The actual slope threshold will depend on sensing range. The default value of SLP\_THD[7:0] is 0x14.

RANGE[3:0]	Sensing Range	Actual Slope Threshold (mg)
4'b0011	±2g	SLP_THD[7:0] * 3.91
4'b0101	±4g	SLP_THD[7:0] * 7.81
4'b1000	±8a	SLP_THD[7:0] * 15.63

**SIGMOT1** Register (29h)

	10910101 (=011	7			400		MINE WITH	
b7	b6	b5	b4	b3		b2	b1	b0
			SKIP_T	TME[7:0]	AW			
			8'b100	010110				
		•	R	/W			,	

This register is used to set the skip time for the significant motion. Holding the duration for skip, for which the motion is checked for re-detection. 1 LSB=20 ms. Range is 0 to 10sec. The default value of SKIP\_TIME[8:0] is 0x96 correspond to 3 seconds.

**SIGMOT2** Register (2Ah)

	<u></u>			icological cological color			
b7	b6	b5	b4	b3	b2	b1	b0
		reserved			ANY_MOT_EN	SIG_MOT_EN	SKIP_TIME[8]
		5'b00000	4 Y		0	1	0
		RO			R/W	R/W	R/W

This register contains MSB of SKIP\_TIME[8:0] for the significant motion, and significant motion interrupt enable bit.

BIT	BIT NAME	Description
1	SIG_MOT_EN	0 : Disable significant motion. 1 : Enable significant motion.
2	ANY_MOT_EN	0 : Disable any-motion. 1 : Enable any-motion.

**SIGMOT3** Register (2Bh)

b7	b6	b5	b4	b3	b2	b1	b0	
reserved			P	ROOF_TIME[7:0				
0			7'b0110010					
RO			R/W					

This register is used to set the proof time for the significant motion. Holding the duration for proof, for which the motion is re-checked after. 1 LSB=20 ms. Range is 0 to 2.5sec. The default value of PROOF\_TIME[7:0] is 0x32 correspond to 1 seconds.

**PRIMIF** Register (33h)

1000									
b7 b6 b5 b4 b3 b2 b1 b0									
SPI_PRIMARY[7:0]									
8'b0000000									
	R/W								

This register is used to set primary communication interface. Write 0x5A into SPI\_PRIMARY to set SPI for primary interface.



**INTFCFG** Register (34h)

b7	b6	b5	b4	b3	b2	b1	b0
		reserved	I2C_WDT_EN	I2C_WDT_SEL	SPI_3WM		
5'b00000					0	0	0
RO					R/W	R/W	RO

This register contains the digital interface parameters for the I<sup>2</sup>C or SPI interface.

BIT	BIT NAME		Description
0	SPI_3WM	SPI 3-wire interface activation. 0: 4-wire SPI interface used. 1: 3-wire SPI interface used.	
1	I2C_WDT_SEL	I <sup>2</sup> C watchdog timer period selection. 0: Watchdog timer period 1ms. 1: Watchdog timer period 50ms.	
2	I2C_WDT_EN	I <sup>2</sup> C watchdog timer enable bit. 0 : Disable I2C watchdog timer. 1 : Enable I2C watchdog timer.	

**OFSTCOMP1** Register (36h)

b7	b6	b5	b4	b3	b2	b1	b0		
OFST_RST		reserved							
0		7'b0000000							
W				RO					

This register is used to define the setting for the offset compensation.

BIT	BIT NAME	Description
7	OFST_RST	1 : Reset all the offset compensation register (register 0x38 ~ 0x3A) to zero.

**OFSTX** Register (38h)

	,,		VOISISION.	10100101					
B7	b6	b5	b4	b3	b2	b1	b0		
OFST_X[7:0]									
	8'b00000000								
	RW								

This register contains the offset compensation value for the x-axis data output.

**OFSTY** Register (39h)

В7	b6	b5	b4	b3	b2	b1	b0			
	OFST_Y[7:0]									
	8,P00000000									
	R/W									

This register contains the offset compensation value for the y-axis data output.

**OFSTZ** Register (3Ah)

b7	b6	b5	b4	b3	b2	b1	b0		
	OFST_Z[7:0]								
	8,00000000								
	R/W								

This register contains the offset compensation value for the z-axis data output.

Register 0x38 to 0x3A can be modified manually set by user. The value in these register will be added to the actual acceleration data sensing by STK8325 and store the new value to XOUT/YOUT/ZOUT register.



FIFOCFG1 Register (3Dh)

b7	b6	b5	b4	b3	b2	b1	b0			
reserved		FIFO_WM_LV[6:0]								
0		7'b0000000								
RO		•	•	R/W						

This register contains FIFO watermark level. If the number of unread frames in the FIFO is equal to FIFO watermark level, an interrupt will be triggered. Please note writing to register FIFOCFG1 clears the FIFO buffer and overrun flag, and resets FIFO-full and watermark interrupts. If 0, the FIFO watermark interrupt is disabled.

#### FIFOCFG2 Register (3Eh)

b7	b6	b5	b4	b3	b2	b1	b0	
FIFO_MODE[2:0]			reserved	FIFO_INTE	ERVAL[1:0]	FIFO_DATA_SEL[1:0]		
3'b000			0	2'b	000	2'b	000	
	R/W		RO	R/	W	R/	W	

This register contains FIFO configuration settings. Please note writing to register FIFOCFG2 clears the FIFO buffer and overrun flag, and resets FIFO-full and watermark interrupts.

	Acceptably Valuetation, Valuetation			
FIFO_MODE[2:0]	Mode selection			
3'b000	Bypass mode			
3'b001	FIFO mode			
3'b010	reserved			
3'b011	Stream-to-FIFO mode			
3'b100	Bypass-to-Stream mode			
3'b101	reserved			
3'b110	Stream mode			
3'b111	reserved			

FIFO_INTERVAL[1:0]	FIFO data subsampling interval
2'b00	1
2'b01	2
2'b10	4
2'b11	8

FIFO_DATA_SEL [1:0]	FIFO data source
2'b00	XYZ-axes
2'b01	X-axis only
2'b10	Y-axis only
2'b11	Z-axis only

#### FIFODATA Register (3Fh)

b7		b6	b5	b4	b3	b2	b1	b0
FIFOOUT[7:0]								
	8'b00000000							
	RO							

This register contains FIFO data output. The format of the LSB and MSB components corresponds to that of the acceleration data readout registers (0x02-0x07). The new data flag is preserved. Read burst access may be used since the address counter will not increment when the read burst is started at the address of FIFODATA. The entire frame is discarded when a frame is only partially read out.

Data format depends on the setting of FIFO\_DATA\_SEL[1:0], if X+Y+Z data are selected, the data of frame n is reading out in the order of XLSB(n), XMSB(n), YLSB (n), YMSB (n), ZLSB (n), ZMSB (n); if X-only is selected, the data of frame n and n+1 are reading out in the order of XLSB (n), XMSB (n), XLSB (n+1), XMSB(n+1); the Y-only and Z-only modes behave analogously.



### 10. APPLICATION INFORMATION

### 10.1 New Data Interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after storing a new value of z-axis acceleration data in the data register. The interrupt is cleared automatically when the next cycle of data acquisition starts. The interrupt status is '0' for at least 50µs. The interrupt mode of the new data interrupt is keep to non-latched for at least 250 us to 3ms.

Control Register	Bit Name	Function
INTEN2[4]	DATA_EN	'1': enabled, '0': disabled, and the interrupt mode is fixed to non-latched.
INTSTS[7]	DATA_STS	The interrupt status
INTMAP2	DATA2INT1 DATA2INT2	New data interrupt maps to INT1 or INT2.
DATASETUP[5]	DATA_SEL	'1': unfiltered data, '0': filtered data, as the input of the new data interrupt

### 10.2 Any-motion (Slope) Detection

Any-motion (slope) detection is to detect the change of motion. By monitoring the slop of acceleration, user can estimate the variation of acceleration. STK8325 use the slop between successive acceleration data to detect it, and would active the interrupt when the slop exceeds a preset threshold. Moreover, a duration setting has to be configured to suppress failure signals. The following figure shows the relationship between acceleration data, acceleration slop, and INT status. If a certain number *N* of consecutive slope data points is larger (smaller) than the slope threshold, the INT would be trigger (clear).

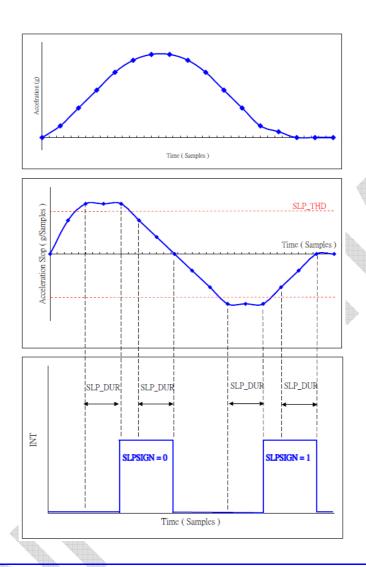
One LSB of SLP\_THD [7:0] represents 1 LSB of acceleration data, and it depends on which sensing range is set. For Example, 3.91mg in 2g-range, 7.81 mg in 4g-range and 15.6 mg in 8g-range. The consecutive slope data points are set by SLP\_DUR [1:0], and is equal to (SLP\_DUR [1:0] + 1). The time difference between the successive acceleration signals depends on the selected bandwidth and equates to 1/(2\*bandwidth).

Any-motion (slope) detection can be enabled by writing '1' to ANY\_MOT\_EN bit in the register <u>SIGMOT2</u> (0x2A). Furthermore, user must select which axes are enabled independently by writing '1' to the bit SLP\_EN\_X, SLP\_EN\_Y, and SLP\_EN\_Z in the register <u>INTEN1</u> (0x16).

If slope of any axis fulfills the specified condition, INT pin would be triggered, interrupt status would be updated to ANY\_MOT\_STS, and the sign of slop would be shown in SLPSIGN\_X, SLPSIGN\_Y, SLPSIGN\_Z. Moreover, SLP\_1ST\_X, SLP\_1ST\_Y, and SLP\_1ST\_Z would indicate which axis is the first axis triggering the interrupt of slop detection.

Control Register	Bit Name	Function	
<u>INTEN1</u> [0]	SLP_EN_X	Slope detection enable for X-axis, '1': enabled, '0': disabled	
<u>INTEN1</u> [1]	SLP_EN_Y	for Y-axis, '1': enabled, '0': disabled	
<u>INTEN1</u> [2]	SLP_EN_Z	for Z-axis, '1': enabled, '0': disabled	
SIGMOT2[2]	ANY_MOT_EN	Any-motion enable bit. 0: Disabled. 1: Enabled.	
SLOPETHD [7:0]	SLP_THD	Slope threshold, 1LSB=1LSB of XOUT/YOUT/ZOUT	
SLOPEDLY [1:0]	SLP_DUR	Slope duration, 1LSB=1/(2*bandwidth)	
INTMAP1	ANTMOT2INT1 ANTMOT2INT2	Slope detection interrupt maps to INT1 or INT2	
INTSTS1 [2]	ANT_MOT_STS	Slope detection status which is synchronized with INT1 or INT2 activity	
DATASETUP [7]	DATA_SEL	'1': unfiltered data, '0': filtered data, as the input of the slop detection	
EVENTINFO1 [0]	SLP_1ST_X		
EVENTINFO1 [1]	SLP_1ST_Y	'1': triggered axis, '0': not triggered	
EVENTINFO1 [2]	SLP_1ST_Z		
EVENTINFO1 [4]	SLPSIGN_X	Sign of slope when interrupt is triggered, '0': Positive, '1': Negative	
EVENTINFO1 [5]	SLPSIGN_Y		
EVENTINFO1 [6]	SLPSIGN_Z		





# 10.3 Significant Motion

The significant motion is defined as some activities that might lead to a change in a user's location. Examples of significant motions are walking or biking, sitting in a moving car, coach or train, etc. Examples of situations that should not trigger significant motion include phone in pocket and person is not moving, phone is on a table and the table shakes a bit due to nearby traffic or washing machine. For more information, please refer to Android Sensor types: <a href="https://source.android.com/devices/sensors/sensor-types.html#significant\_motion">https://source.android.com/devices/sensors/sensor-types.html#significant\_motion</a>.

Significant motion function would be triggered by means of monitoring the slope of acceleration over a period of time. The algorithm will be started when a motion is detected, and generates a signal if another motion is detected after the SKIP\_TIME[8:0] (0x29-0x2A) and within the PROOF\_TIME[7:0] (0x2B). Both 1 LSB of skip time and proof time correspond to 20ms.

The significant motion and slope detection share event-triggered settings including independent XYZ-axes slope enable bit <a href="INTEN1">INTEN1</a> [2:0] (0x16), threshold SLOPETHD [7:0] (0x28), duration SLOPEDLY [1:0] (0x27). User should be noticed that the slope detection has to be enabled before enabling significant motion due to a sharing algorithm engine. Then enable significant motion by writing '1' to SIG\_MOT\_EN bit in register <a href="SIGMOT2">SIGMOT2</a> (0x2A).



Follow the steps below to enable significant motion:

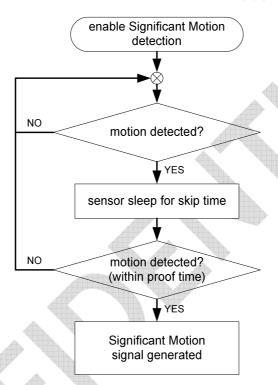
**Step1.** Set configuration settings include SKIP\_TIME[8:0] (0x29-0x2A), PROOF\_TIME[7:0] (0x2B), SLOPEDLY[1:0] (0x27) and SLOPETHD[7:0] (0x28).

**Step2.** Set XYZ-axes slope detection enabled by INTEN1[2:0] (0x16).

Step3. Set significant motion enabled by SIGMOT2[1] (0x2A).

**Step4.** Mapping significant motion to physical interrupt pin by INTMAP1[0] (0x19).

**Step5.** Wait for INT triggered or monitor SIG\_MOT\_STS bit in INTSTS1[0] (0x09)

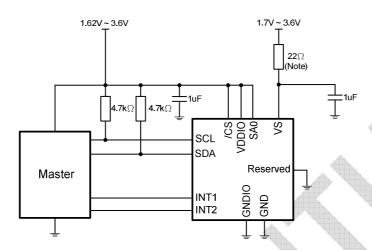


Significant Motion algorithm flow chart

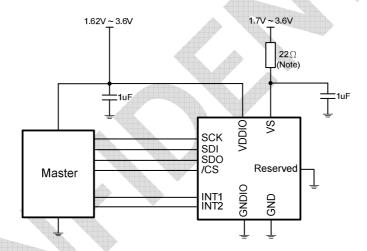


# 10.4 **Application Circuit**

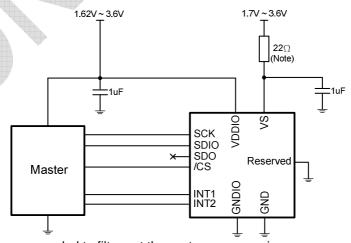
#### I<sup>2</sup>C Interface



#### **SPI 4-wire Interface**



#### **SPI 3-wire Interface**



Note: A 22 ohm resistor is recommended to filter out the system power noise.

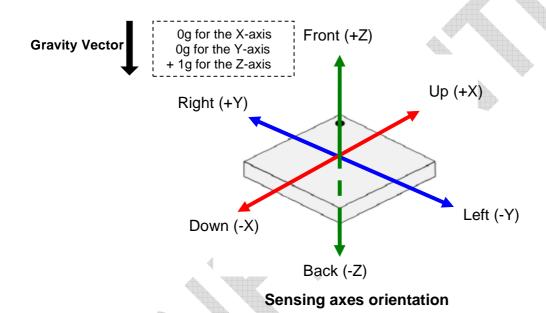


# 10.5 Sensing Axes Orientation

By measuring the acceleration components respect to g field, the position and orientation information could be recognized. It could be used for such applications as Portrait/Landscape in Mobile phone/PDA/PMP. This enables a product to set its display orientation appropriately to either portrait/landscape mode, or to turn off the display if the product is placed upside down. The sensor provides positive or negative directions of X/Y/Z axes. The relationship between directions and six different positions: Left, Right, Up, Down, Back, and Front, is shown in the following figure.

If the sensor is at rest and the force of gravity is acting along the indicated directions, the output of the corresponding channel will be negative (static acceleration).

Example: If the sensor is at rest or at uniform motion in a gravity field according to the figure given below, the output signals are:



The following table lists all corresponding output signals on X, Y, and Z while the sensor is at rest or at uniform motion in a gravity field under assumption of a ±2g range setting, a 12 bit resolution, and a top down gravity vector as shown above.

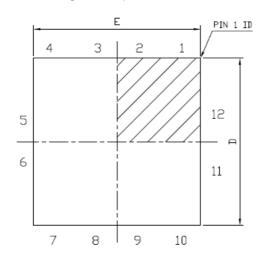
Sensor Orientation & Gravity Vector	Top View	Top View	Top View	Top View	Top bottom Side View	wonog do_L Side View
X-axis Output	+1g/1024LSB	0g / 0 LSB	-1g/1024LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB
Y-axis Output	0g / 0 LSB	+1g/1024LSB	0g / 0 LSB	-1g/1024LSB	0g / 0 LSB	0g / 0 LSB
Z-axis Output	0g / 0 LSB	+1g/1024LSB	-1g/1024LSB			

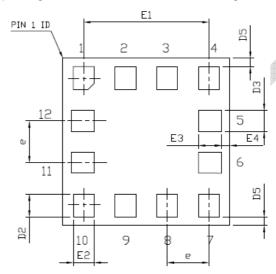


# 11. PACKAGE OUTLINE

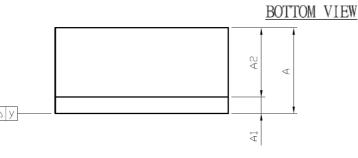
# 11.1 Package Outline Drawing

The sensor housing is a 12-pin 2.0mm x 2.0mm x 1.0mm LGA package. Its dimensions are the following.





TOP VIEW



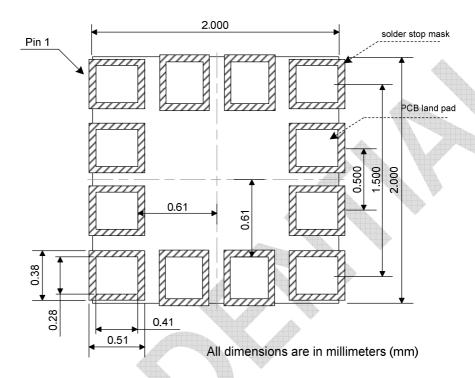
SIDE VIEW

CONTROL CONTRO	V				
SYMBOLS	DIMENS	DIMENSIONS IN MILLIMETERS			
STIVIDULS	MIN.	MIN. NOM.			
Α	0.95	1.00	1.05		
A1		0.20 REF.			
A2		0.80 REF.			
D	1.95	2.00	2.05		
D2	0.225	0.275	0.325		
D3	0.20	0.25	0.30		
D5		0.10			
Е	1.95	2.00	2.05		
E1		1.50			
E2	0.20	0.25	0.30		
E3	0.225	0.275	0.325		
E4		0.10			
Е		0.50			
Y	0.00		0.10		



# 11.2 Recommended PCB Layout

The PCB layout should use NSMD (Non Solder mask Defined) pad definitions for all pads.

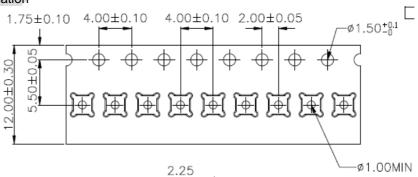


# 11.3 Marking Rule

Marking	Symbol	Name
YYYY	YYYY	Order number
XXXX	XXXX	Product serial number
•	•	Pin1 dot

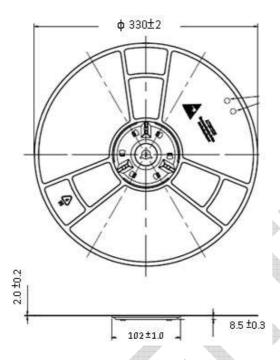
# 11.4 Tape and Reel Information

#### 1. Carrier Tape Specification

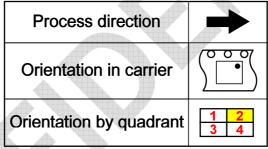




#### 2. Reel Specification

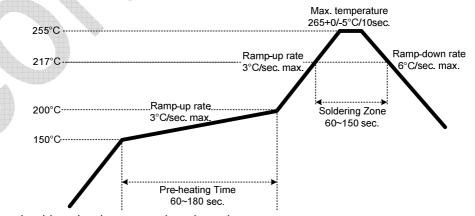


#### 3. Unit Orientation



# 11.5 Soldering Condition

1. Pb-free solder temperature profile



- 2. Reflow soldering should not be done more than three times.
- 3. When soldering, do not put stress on the ICs during heating.
- 4. After soldering, do not warp the circuit board.

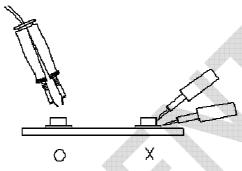


## 11.6 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350°C for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

### 11.7 Repairing

Repair should not be done after the ICs have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the ICs will or will not be damaged by repairing.



### 12. STORAGE INFORMATION

# 12.1 Storage Condition

- 1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
- 2. The delivery product should be stored with the conditions shown below:

Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

## 12.2 Treatment After Unsealed

1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be rebaked before reflow to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours



**Revision History** 

Date	Version	Modified Items
2019/07/30	1.0	Initial release.
2019/11/12	1.1	Update recommended PCB layout.
2020/04/28	1.2	Update SPI timing.
2020/10/15	1.3	<ol> <li>Update tape and reel information.</li> <li>Fix Typo.</li> </ol>

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